DESIGN OF CAD TOOL FOR BOOLEAN FUNCTION MINIMIZATION

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Abstract

Use of computer-aided design tool are preferred in digital systems design not only because they are time saving but for the flexibility they offer-the accurate and more comprehensive performance evaluation studies possible by varying input variables over a wide range and under different operating constraints. This paper presents the design and implementation of a digital systems design tool intended for use primarily in a critical study of the Quine-McCluskey tabulation method of minimizing Boolean functions. However, it has also doubled as a handy CAD package for the teaching of this minimization technique to students of Electronic and Computer Engineering. The software models this reduction process for up to twenty six variables, allowing the user to adjust his selections in somewhat fuzzy situations and then assess the effect on the final digital logic function each derives. A graphic interface renders the minimized expression as a digital logic circuit diagram. The CAD tool assists the digital system designer not only in the process of minimization but also in reliability and cost estimates.

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